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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/587,079	07/21/2006	Norikatsu Takaura	XA-10616	9411

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EXAMINER	
LAURENZI, MARK A	

ART UNIT	PAPER NUMBER
2894	

NOTIFICATION DATE	DELIVERY MODE
02/19/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/587,079	TAKAURA ET AL.	
	Examiner	Art Unit	
	MARK A. LAURENZI III	2894	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the arguments/remarks correspondence filed 10-02-2009.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2 and 11 in part, recite the limitation "the group b". In the instant case it is not clear if the limitation "the group b" refers to the (deleted) limitations of claim 1 or other limitations not present within the recitation. There is insufficient antecedent basis for this limitation in the claim.

Claims 6 and 15 in part, recite the limitation "the layer of the memory layer containing Zn or Cd. In the instant case it is not clear if the limitation "the layer of the memory layer containing Zn or Cd" refers to the limitations found in claim 10 or other limitations not present within the recitation. There is insufficient antecedent basis for this limitation in the claim.

Product by Process Limitations

Initially, and with respect to claim(s) 5 and 14, note that a "product by process" claim is directed to the product per se, no matter how actually made. See In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) and the related case law cited therein which makes it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. As stated in Thorpe, even though product-by-process claims are limited by and defined by the

process, determination of patentability is based on the product itself. In re Brown, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972); In re Pilkington, 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969); Buono v. Yankee Maid Dress Corp., 77 F.2d 274, 279, 26 USPQ 57, 61 (2d. Cir. 1935).

Note that Applicant has burden of proof in such cases as the above case law makes clear.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 4-6, 10-11 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ovshinky 2004/0178402 A1.

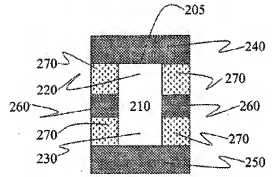

FIG. 3

Re claims 1-2, 4, 6, 10-11 and 15, Ovshinsky (e.g. all relevant Figs. and relates text) teaches: a memory device including a memory element comprising: a memory layer containing at least one element selected from the group consisting of Ge, Sb, and Bi (Ge, one or more from column IV, [0031]), Te (Te, the most common chalcogenide, [0032]) and at least one element

selected from Zn…Cd (transition metals may be modifiers, Zn and Cd, [0032]) and storing information by causing reversible phase-change between a crystal phase and an amorphous phase (crystalline and amorphous states, Abstract); and an electrode formed on both surfaces of the memory layer (240 and 250) *but is explicitly silent with respect to*: where the at least one element selected from the group consisting of contains 2 at% or more and less than 25 at%, 40 at% or more and 65 at% or less of Te and 20 at% or more and 50 at% or less of the at least one element selected from Zn….Cd.

One of ordinary skill in the art would recognize that a memory layer contains an atomic% and that atomic% is a result effective variable.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to optimize the result effective variable i.e. atomic% so as to facilitate for provision of operability in accordance with and in the form of routine experimental optimum workable ranges, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233 (1955).

Re claims 5 and 14, Ovshinsky *is explicitly silent with respect to* a memory device according to claim 1, wherein the memory device is used within an atmosphere at 145°C or higher.

Regarding claims 5 and 14, Ovshinsky teaches all the limitations of the claimed invention yet *remains explicitly silent with respect to* the method of operating a memory device within an atmosphere at 145°C or higher. However, the method of operation is not a structural limitation and does not affect final structure of the claimed invention (a device).

In the instant case, a device or apparatus operating at a temperature lower than 145°C or higher has the same functionalities and/or capabilities of a device that operates at 145°C or higher (See MPEP 2173.05(p)).

Claims 8 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ovshinky 2004/0178402 A1, and further in view of Kinoshita U.S. 4,475,178.

Re claims 8 and 17, Ovshinsky (e.g. all relevant Figs. and relates text) teaches: a memory device comprising: a plurality of memory cells (replication is obvious); wherein each of the plurality of memory cells includes: a memory layer containing Ge or Sb (Ge, one or more from column IV, [0031]), Te (Te, the most common chalcogenide, [0032]), at least one element selected from Zn… Cd (transition metals may be modifiers, Zn and Cd, [0032]), and recording information by causing reversible phase-change between a crystal phase and an amorphous phase (crystalline and amorphous states, Abstract); and electrodes (240 and 250) formed so as to sandwich the memory layer therebetween for applying a voltage to the memory layer *but is explicitly silent with respect to* a plurality of word lines for selecting the plurality of memory cells; a plurality of data lines arranged orthogonally to the plurality of word lines and reading signals from the plurality of memory cells; and where Te is at 40 at% or more and where at least one selected from is at 20 at% or more and 50 at% or less.

However, Kinoshita (e.g. all relevant Figs. and relates text) teaches: a plurality of data lines DL arranged orthogonally to the plurality of word lines WL and reading signals from the plurality of memory cells (Fig. 4).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the memory device including electrodes as taught by Yamada in

view of Kozicki with the word line and date line wiring as taught by Kinoshita for the benefit of forming a memory device that can operate controlled under various design orientations so as to expand the versatility and ease of manufacturing said device.

Yet, Ovshinsky in view of Kinoshita *remain explicitly silent with respect to* where Te is at 40 at% or more and where at least one selected from is at 20 at% or more and 50 at% or less.

One of ordinary skill in the art would recognize that a memory layer contains an atomic% and that atomic% is a result effective variable.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to optimize the result effective variable i.e. atomic% so as to facilitate for provision of operability in accordance with and in the form of routine experimental optimum workable ranges, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233 (1955).

Claims 9 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ovshinky in view of Kinoshita as applied to claims 8 and 17 above, and further in view of Yamada et al. 5,278,011.

Re claims 9 and 18, Ovshinsky in view of Kinoshita *is explicitly silent with respect to* a memory device according to claim 8, wherein an insulating film is disposed between the memory layer and one surface of the electrode.

However, Yamada (e.g. all relevant Figs. and relates text) teaches a dielectric layer 2/3 situation upon a memory layer 4 (Fig. 1A).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the semiconductor device as taught by Ovshinsky with an insulation memory layer configuration as taught by Yamada for the benefit of making the resistively of the between the electrodes adjustable so as to maximize performance of the device.

Claims 3 and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ovshinky as applied to claims 1 and 10 above, and further in view of Schneider 6,625,848 B1.

Re claims 3 and 12, Ovshinsky *is explicitly silent with respect to* a memory device according to claims 1 or 10, wherein said one element selected from Zn….Cd is partially or entirely replaced with nitrogen.

However, Schneider (e.g. all relevant Figs. and relates text) teaches a shape memory alloy (SMA) (col. 1/lls. 14-15) and that an SMA element may include Cd, Zn and nitrogen (col. 5/lls. 10-14).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the semiconductor device including a memory region as taught by Ovshinsky with the memory element as taught by Schneider for the benefit of in part of providing a consistent performance to a semiconductor device (col. 2/lls.33-34).

Re claim 13, all of the limitations of claim 13 are met by Ovshinsky as applied to claim 10 above except where at least one element selected from Zn... Cd further includes nitrogen.

However, Schneider (e.g. all relevant Figs. and relates text) teaches a shape memory alloy (SMA) (col. 1/lls. 14-15) and that an SMA element may include Cd, Zn and nitrogen (col. 5/lls. 10-14).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the semiconductor device including a memory region as taught by Ovshinsky with the memory element including nitrogen as taught by Schneider for the benefit of in part of providing a consistent performance to a semiconductor device (col. 2/lls.33-34).

Claim 7 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ovshinky as applied to claims 1 and 10 above, and further in view of Morikawa et al. 5,644,416.

Re claims 7 and 16, Ovshinsky *is explicitly silent with respect to* a memory device according to claims 1 and 10, wherein the memory device transmits 30% or more of recording light or reading light.

However, Morikawa (e.g. all relevant Figs. and relates text) teaches: an optical memory system where information is read and written by light. Furthermore, Morikawa teaches light of longer wavelength is preferred (col. 1/lls. 48-65).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the semiconductor device including a memory region as taught by Ovshinsky with the optical memory system as taught by Morikawa for the benefit manufacturing a semiconductor device having excellent stability while having simple construction (Morikawa, col. 2/lls. 49-51).

Yet, Ovshinsky in view of Morikawa *remain explicitly silent with respect to* where the memory device transmits 30% or more of light.

One of ordinary skill in the art would recognize that optical memory system has transmitting properties and that light transmission is a result effective variable.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to optimize the result effective variable i.e. light transmission so as to facilitate for provision of operability in accordance with and in the form of routine experimental optimum workable ranges, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233 (1955).

Response to Arguments

Applicant's arguments filed 10-20-2009 have been fully considered but are moot in view of the present ground(s) of rejection.

Furthermore, the entirety of Applicant's arguments is addressed by rejection supra.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MARK A. LAURENZI III whose telephone number is (571)270-7878. The examiner can normally be reached on Monday through Friday 8am to 5pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly Nguyen can be reached on 571-272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MARK A. LAURENZI III/
Examiner, Art Unit 2894

/Kimberly D Nguyen/
Supervisory Patent Examiner, Art Unit 2894

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